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A Low Noise PLL Frequency Synthesizer in 2.4 GHz with 1MHz Frequency Step

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Abstract: - *A PLL frequency synthesizer with the frequency span of 2.3-2.5GHz with 1MHz frequency step and phase noise of -90dBc/HZ at 100 KHZ, -130dBc/Hz at 1MHz and -60dBm suppression of spurs level is presented. Basically a practical PLL synthesizer includes a voltage controlled oscillator, a main synthesizer IC and a loop filter. In the first section the introduction is presented, general block diagram is illustrated in the second section, in the next section the blocks are described separately, also loop filter design and frequency setting board are analyzed in the rest and finally conclusion will be presented.*
Key words: - *Synthesizer, PLL, Frequency divider, Loop filter, Phase noise*

I. Introduction

Today the PLL is one of the most common used methods in transceiver equipment. It is extremely used in all forms of radio communication, wireless communication and ….

PLL frequency synthesizer has so many benefits for using local oscillators. They present both high levels of stability and accuracy. They are now being applied to analogue and digital systems. In [1] a frequency synthesizer for fast frequency hopping is used for transceivers in S band. In [2] modeling of a low phase noise synthesizer with an acceptable phase noise is presented (-123 dBc/Hz at 1MHz step frequency). An output of -90dBc/Hz with an output power of -10dBm achieved in [3] also a low spurs level with a low output power has been presented in [4].

In this paper design and construction of a frequency synthesizer based on PLL method with an acceptable specifications such as low phase noise, low spurious output and the ability to step 1 MHZ in S band is presented.

II. General Block Diagram

Generally the PLL contains several blocks. As shown in figure 1, the blocks in a PLL frequency synthesizer are:

A voltage control oscillator (VCO), phase comparator, loop filter, crystal reference oscillator, and finally programmable divider [5], [6].

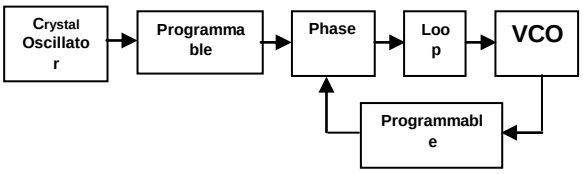

Fig.1: General Block Diagram of a PLL Synthesizer

The basics of PLL is comparing of two signals, one of them comes from reference oscillator and another one comes from VCO, then they are compared by phase comparator and the phase difference between these two input signals is produced. The produced phase difference signal is then passed through the loop filter that suppresses any unwanted signal, after that it is applied to the VCO. This voltage tries to reduce the error between two signals entering the phase comparator.

So, the frequency of VCO will be changed to the reference then is locked, after the PLL locked, input and output frequencies will be equal.

$$\mathbf{f_O = \frac{n}{R} f_R} \qquad (1)$$

In above equation, f_R is reference frequency, f_O is output frequency then with selecting suitable amount of n and R, the requested frequency can be set.

Usually several frequency divider is used on the path of VCO to phase detector feed back to have more flexibility in setting output frequency. A more detailed block diagram is shown in figure 2.

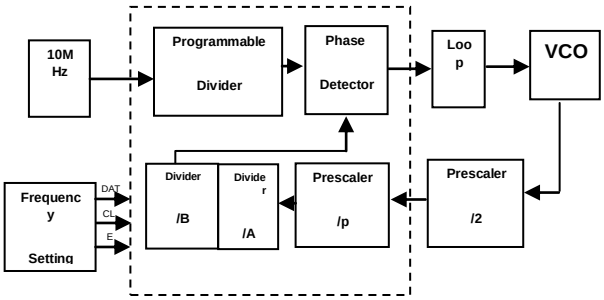

Fig.2: Detailed Block diagram

III. Description of the blocks:

a) Voltage control oscillator (VCO):

The VCO in which is used to realize the circuit is JTOS-3000 [7]. It is able to oscillate between 2-3 GHZ. A 5v power supply is provided by a 9v of voltage regulator. Its output level is 10 dBm. The variation of 5v to 12v can produce the frequency range between 2-3 GHz; the higher frequency can be selected by increasing the tune voltage amount.

$$F_{VOC} = \frac{2(P*B+A)}{R} * F_R \qquad (2)$$

F_R is reference frequency, F_{VCO} is voltage control oscillator frequency, A and B are coefficient of programmable divider and P is coefficient of prescaler of the divider. (2)

As shown in figure 3, the synthesizer can be used in a transceiver. VCO has two outputs: One of them is applied to a receiver to down-convert the frequency demodulation of the signal, and another output goes to transmitter for signal modulation.

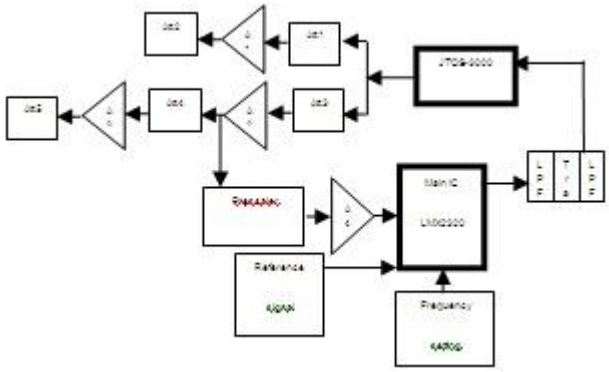

Fig.3: The Complete Block diagram of a transceiver using PLL synthesizer

b) RF attenuators and Amplifiers:

The configuration of attenuator is π & T type [8]. These attenuators are used for two purposes; First, to control the signal power level. Second, to improve and facilitate the matching between different stages.

Design of a typical attenuator with π configuration comes in the figure 4.

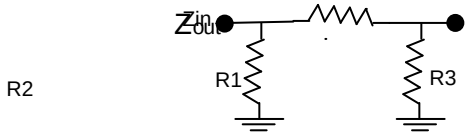

Fig.4: π configuration resistive attenuator

$$R_3 = 1/2\,(10^{L/10} - 1)\,[(Z_{in} \times Z_{out}) / 10^{L/10}]^{1/2}$$
$$R_2 = 1/[(10^{L/10} + 1) / Z_{out}(10^{L/10} - 1)] - 1/R_3$$
$$R_1 = 1/[(10^{L/10} + 1) / Z_{in}(10^{L/10} - 1)] - 1/R_3$$

Where L is desired loss in dB, Z_{in} and Z_{out} are input and output impedance in Ω, respectively.

The more information exists in every attenuator design tutorial or the standard table of resistive attenuators. In our design a 10 dB attenuator with 50Ω input and output impedance is used in the receiver path and has the following configuration (Figure 5):

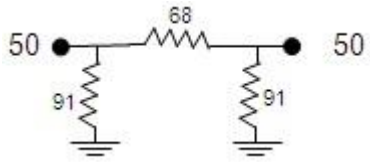

Fig.5: A 10dB Attenuator

A couple of amplifiers are used in the transmitter and receiver path to increase the power level of driving. Because driving the transmitter and receiver inputs need to increase the power level of VCO. To realize this, two types of amplifiers are used: SGA 4586 and UPC 2711T [9].

As it is clear in figure 3, the output of VCO is divided to two branches: one of them is applied to receiver by amplifying with SGA4586 [10]. The output level in this branch is 3dBm which applied to receiver and is flexibly controlled by the amount of attenuation. Another branch after amplification with the same amplifier is divided to two parts again: one path is applied to transmitter, then -20dB attenuation is done by two π configuration attenuator that each one has 10dB. Another path with amount of -5dB attenuation is applied to a prescaler (UPB 584G) [9] by π configuration attenuator. The output frequency will be divided to 2 (i.e.: 1.2 GHZ). Then an amplification is provided by RF power amplifier UPC 2711T to phase comparison stage.

c) Main IC of synthesizer:

Now, we analyze the most important part namely main IC of synthesizer. For this purpose, the famous series of LMX 2320 is used as shown in figure 6 [11].

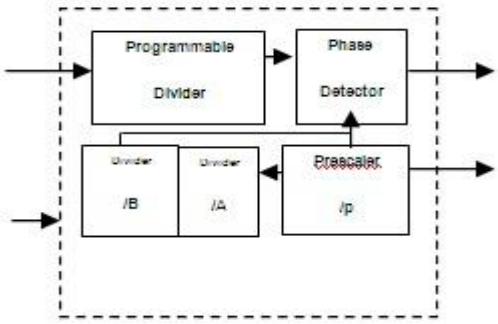

Fig.6: The Functional Block diagram of LMX 2320

This IC includes different blocks: a phase comparator, a prescaler, and three programmable frequency dividers. The 10MHz basic signal produced by a stable crystal oscillator is applied to LMX 2320. The output signal coming from VCO after being divided to 2 by an external prescaler (UPB 584G) is compared with the reference signal by phase comparator. The output DC voltage of comparator will be applied to the external loop filter.

The LMX2320 also includes prescaler and programmable dividers that are controlled by a frequency setting section. We used a CPLD which will be described later.

IV. Loop filter

Low phase noise, spurious and frequency stability are major goals in design of a PLL frequency synthesizer. These characteristics largely depend on the loop filter. The simplified loop-filter design formulas, can be found in PLL Application Guide of Fujitsu are detailed [12]. The formulas are based on the use of a basic passive two-pole loop filter along with a single pole spur filter. The necessary information for calculation of loop filter components are:

1- **The ratio of frequency to relative voltage of VCO [K_{VCO} (MHZ/V)]**
2- **VCO output frequency (F_{opt} (MHZ))**
3- **Ratio of output current to input phase difference.**
4- **Input frequency to phase detector [F_{ref}(KHZ)]**

Also other information to design more accurate can be derived from Datasheet of LMX2320 [11]. The configuration of loop filter is shown in figure 7.

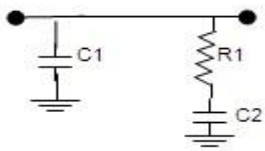

Fig.7: Loop Filter

According to datasheet of main IC [11] and also VCO [7], parameters can be obtained as following: From [7] K_{VCO} = 50 – 150 MHz**,** then we choose K_{VCO} = 100MHz/V, From [11] we have K_{φ} =5mA, , F_{opt} = 1200MHZ and F_{ref} = 250KHZ ,then we calculate parameters as following: **C_1=20nf R_1=390Ω C_2=94nf** Because of comparing frequency in the phase detector is 250 KHZ, output has spurs. It is important to remove these spurs from output. For this reason, a LPF along with a trap is predicted after the loop filter. The configuration is shown in figure 8:

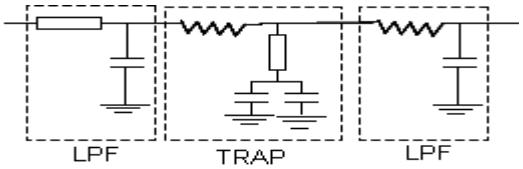

Fig.8: LPF and Trap for 250KHZ

Also an extra LPF for damping high frequency noises is used in the third stage.

V. Alarm

If PLL circuit faces the fault in frequency locking, the lock detection pine of LMX 2320 will turn off, and the comparison circuit will produce an alarm, finally LED will turn on.

VI. Frequency setting Board

In this sketch we used CPLD from Xilinx XC9572XL [13] to simplify and miniaturize the digital board and minimizing noise effect and as well as save energy. Foundation software with version 2.1 is used to program the CPLD. There are two methods to program: HDL and schematic. In this sketch we used second method. The frequency set contains three parts: clock generator, shift register and power reset. The clock generator part used of IC, and the power reset is MPC 2270. The shift register section includes five 74HC166 IC. The parallel data coming from a BCD switch to IC parallel input with applying clock to pin 6 of IC will change to serial.

So the necessary data for the next stage (LMX 2320) will be provided.

VII. Results Analysis

The constructed PLL synthesizer can operate between 2.3-2.5GHZ with step frequency of 1 MHZ.
The phase noise for different frequencies is:

-60 dBc/ HZ 1KHz offset
-75 dBc/Hz 10 KHz offset
-90 dBc/Hz 100 KHz offset
-130 dBc/Hz 1MHz offset

The damping of spurses is up to-60dBm and second Harmonic is -30dBm.
We should remove the spurs in shown in figure 9:

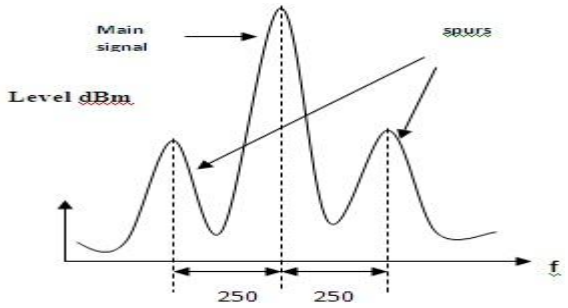

Fig.9**:** The main signal with two spurs

Finally figure 10 illustrates the ideal spectrum without any spurs.

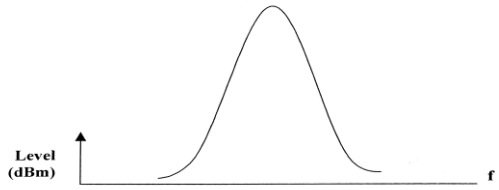

Fig.10: suppression of spurs

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